Docket No. 244838US2S

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Takashi YAMADA, et al.

SERIAL NO: New Application GAU:

FILED: Herewith EXAMINER:

FOR: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

Applicant(s) wish to disclose the following information.

REFERENCES

■ The applicant(s) wish to make of record the references listed on the attached form PTO-1449. Copies of the listed references are attached, where required, as are either statements of relevancy or any readily available English translations of pertinent portions of any non-English language references.

☐ A check or credit card payment form is attached in the amount required under 37 CFR §1.17(p).

RELATED CASES

■ Attached is a list of applicant's pending application(s) or issued patent(s) which may be related to the present application. A copy of the patent(s), together with a copy of the claims and drawings of the pending application(s) is attached along with PTO 1449.

☐ A check or credit card payment form is attached in the amount required under 37 CFR §1.17(p).

CERTIFICATION

☐ Each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.

☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

DEPOSIT ACCOUNT

■ Please charge any additional fees for the papers being filed herewith and for which no check or credit card payment is enclosed herewith, or credit any overpayment to deposit account number 15-0030. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

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LIST OF RELATED CASES

Docket Number	Serial or Patent Number	Filing or Issue Date	Inventor/ Applicant
PER CLIENT	10/407,677	04/07/03	NAGANO et al.
PER CLIENT	10/237,206	09/09/02	NAGANO et al.
PER CLIENT	10/439,896	05/16/03	NAGANO et al.
216692US2	09/995,594	11/29/01	YAMADA et al.
219723US2S	10/078,344	02/21/02	NAGANO et al.
220111US2S	6,531,754	03/11/03	NAGANO et al.
220473US2S	6,630,714	10/07/03	SATO et al.
220753US2S	10/096,655	03/14/02	YAMADA et al.

*Present Application; listed for information

EHK/sb

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IN RE APPLICATION OF: Takashi YAMADA, et al.

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FOR: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

STATEMENT OF RELEVANCY

Reference AM (JP 10-303385) on Form PTO- 1449:

Fig. 1 shows device fabrication on a hybrid substrate of SOI region and bulk region. Stacked DRAM cell is formed in the bulk region.

Reference AN (JP 8-316431) on Form PTO- 1449:

Fig. 1 shows device on a hybrid substrate of SOI region and bulk region. Fig. 3 - 23 shows the fabrication process. Stacked DRAM cells are formed in the SOI region.

Reference AO (JP 7-106434) on Form PTO- 1449:

This shows device fabrication on a hybrid substrate of SOI region and bulk region. Stacked DRAM cells are formed in the bulk region.

Reference AP (JP 11-238860) on Form PTO- 1449:

This shows device fabrication on a hybrid substrate of SOI region and bulk region. Stacked DRAM cells are formed in the bulk region.

Reference AQ (JP 2000-91534) on Form PTO- 1449:

This shows device fabrication on a hybrid substrate of SOI region and bulk region. Stacked DRAM cells are formed in the bulk region.

Reference AR (JP 2000-243944) on Form PTO- 1449:

This shows fabrication process of hybrid substrate using epitaxial growth technique.

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IN RE APPLICATION OF: Takashi YAMADA, et al.

SERIAL NO: New Application

FILED: Herewith

FOR: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

STATEMENT OF RELEVANCY

Reference AS (JP 8-17694) on Form PTO- 1449:

This shows fabrication process of hybrid substrate using epitaxial growth technique.

Reference AT (JP 11-17001) on Form PTO- 1449:

This shows fabrication process of hybrid substrate using epitaxial growth technique.

Form PTO 1449 (Modified)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY DOCKET NO.	SERIAL NO.
		244838US2S	New Application
LIST OF REFERENCES CITED BY APPLICANT		APPLICANT	
		Takashi YAMADA, et al.	
		FILING DATE	GROUP
		Herewith	

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA	6,531,754	03/11/03	Hajime NAGANO, et al.			
	AB	6,630,714	10/07/03	Tsutomu SATO, et al.			
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES	TRANSLATION NO
	AM	10-303385	11/13/98	Japan		x
	AN	8-316431	11/29/96	Japan		x
	AO	7-106434	04/21/95	Japan		x
	AP	11-238860	08/31/99	Japan		x
	AQ	2000-91534	03/31/00	Japan		x
	AR	2000-243944	09/08/00	Japan		x
	AS	8-17694	01/19/96	Japan		x
	AT	11-17001	01/22/99	Japan		x

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)

	AU	Robert HANNON, et al., "0.25 μm Merged Bulk DRAM and SOI Logic using Patterned SOI", SYMPOSIUM ON VLSI TECHNOLOGY DIGEST OF TECHNICAL PAPERS, 2000, pgs. 66-67
	AV	H. L. HO, et al., "A 0.13 μm High-Performance SOI Logic Technology with Embedded DRAM for System-On-A-Chip Application", IEDM TECH. DIG., 2001, pgs. 503-506
	AW	T. YAMADA, et al., "An Embedded DRAM Technology on SOI/Bulk Hybrid Substrate Formed with SEG Process for High-End SOC Application", SYMPOSIUM ON VLSI TECHNOLOGY DIGEST OF TECHNICAL PAPERS, 2002, pgs. 112-113
	AX	Hajime NAGANO, et al., "SOI/Bulk Hybrid Wafer Process Using SEG (Selective Epitaxial Growth) Technique for High-End SoC Applications", EXTENDED ABSTRACTS OF THE 2002 INTERNATIONAL CONFERENCE ON SOLID STATE DEVICES AND MATERIALS, 2002, pgs. 442-443
	AY	Takashi YAMADA, et al., "An Embedded DRAM Technology in SOI for High-End SoC Application", SEMI TECHNOLOGY SYMPOSIUM, 2002, pgs. 2-39-2-44 (with English Abstract)
	AZ	☐ Additional References sheet(s) attached

Examiner	Date Considered

*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.